IN THE SPECIFICATION

Please insert before the first paragraph under BACKGROUND OF THE INVENTION of page 1 of the disclosure currently on file with the following paragraph:

This application is a Continuation of nonprovisional U.S. application serial number 10/287,678 filed November 5, 2002. Priority is claimed based on U.S. application number 10/287,678 filed November 5, 2002, which claims the priority of Japanese application 2001-338938 filed on November 5, 2001.

Amendments to the Specification:

Please replace paragraph [0002] with the following amended paragraph:

DRAMs are generally used to reduce the area of a chip and hence minimize the manufacturing costs thereof. Fig. 9A shows a single-intersection memory cell array having memory cells connected at all intersections of word lines WL (WL0, WL1, WL2) and bit lines BL (BL0B, BL0T, BL1B, BL1T, BL2B, BL2T). Compared with known dual-intersection memory cell arrays having memory cells connected at only half of the intersections of word and bit lines, the area occupied by the single-intersection memory cell array can be reduced by 25%. Referring to Fig. 9A, there are shown sense amplifiers SA0, SA1, SA2, etc.

Please replace paragraph [0006] with the following amended paragraph:

Where the amount of intelligence on the bit line BL1T has substantially decreased due to current leakage or any other reason, the signals with a large amount of intelligence on the bit lines BL0 and BL2 are amplified first. As indicated by dotted arrows in Fig. 9A, a potential difference between the bit line BL0 (BL0T, BL0B) or BL2 (BL2T, BL2B) and the bit line BL1 (BL1T, BL1B)brings about a potential difference between the word line WL0 and an adjoining one WL1, WL2 or WL3 due to a parasitic capacitor CBLWL formed between a bit line and word line. The potential difference returns to the bit line BL1 via the parasitic capacitor CBLWL.

Please replace paragraph [0032] with the following amended paragraph:

After the pre-charging of the sense amplifiers SA is terminated, a sub-word driver SWD activates the word line WL0 so as to read data items from the memory cells MC onto bit lines BL0T, BL1T . . . BL510T, BL511T, etc. The sense amplifiers SA amplify the differences between weak signals developed on the bit lines and reference potentials on side-B bit lines BL0B, BL1B . . . BL510B, BL511B, etc., and hold the results.

Please replace paragraph [0034] with the following amended paragraph:

A Pre-fetch command PFC is then issued, whereby the data items in the sense amplifiers SA are transferred to data registers RE over main input/output lines MIO. At this time, either of the groups of memory cells MCB0 and MCB1 is selected based on a group selecting signal BSL (BSL0, BSL1), and the data items held in the selected bank are transferred simultaneously to the data registers RE. When the data items are written in the registers RE over the main input/output lines, encoders EN constituting an encoder bank ENB decode the data items as described below.

Please replace paragraph [0041] with the following amended paragraph:

When data items RE-T and RE-B are read from the data registers RE into the sense amplifiers SA during restoring, the number of 0s among all the bits of data items stored in the group of memory cells MCB0 is normally larger than the number of 1s. If, however, the number of 1s wins a majority, a 1 is written in the flag register FRE in order to invert the data items. The encoding is realized when the encoder bank ENB inverts values written in the data registers RE and transfers the resultant values to the sense amplifiers SA over the main input/output lines MIO. When the number of 1s is one-half or less than one-half of the sum total of bits, the values in the data registers RE are not inverted but transferred to the sense amplifiers SA as they are.

Please replace paragraph [0044] with the following amended paragraph:

Fig. 1B shows the effect in minimizing the array noise that occurs in the encoding DRAM of this first preferred embodiment of the present invention. When encoding is not performed (NO ENCODING), 512 bits on the word lines WL0 (WL0 IN TOTAL) may be all 0s or 1s and results in the largest array noise (PROBABLE RANGE). The magnitudes of the array noises in the two states are nearly equal to each other and the polarities thereof are opposite to each other. The array noises in such states are defined as the array noises of 100% and -100%. Herein, the bit lines BLF over which the flag memory cells are interconnected are excluded.

Please replace paragraph [0045] with the following amended paragraph:

In contrast, in the DRAM of the present invention (PRESENT INVENTION WITH ENCODING), the number of 1s in the group of memory cells MCB0 is 0 at minimum and 128 at maximum. The number of 1s in the group of memory cells MCB1 is 128 at minimum and 256 at maximum. The sum total of 1s on the word line WL0 (WL0 IN TOTAL) is therefore limited to a range from 128 to 384.

Please replace paragraph [0059] with the following amended paragraph:

The data register RE consists mainly of inverters IV1 and IV2 whose input/output terminals are connected to each other, and a bi-directional switch comprising clocked inverters CIV1 to CIV4. The clocked inverters CIV1 and CIV3 that are controlled with a restoring signal RS have the input terminals thereof connected to internal nodes REI0B and REI0T of the data register and have the output terminals thereof connected to the output nodes RE0T and RE0B thereof. The clocked inverters CIV2 and CIV4 that are controlled with a pre-fetching signal PF have the input terminals thereof connected to the output nodes RE0T and RE0B of the data register and have the output terminals thereof connected to the internal nodes REI0B, ~~and~~ REI0T, REI1B, REI1T . . . REI255B, REI255T thereof. During pre-fetching, the pre-fetching signal is activated and data items on the main input/output lines MIO (MIO0T, MIO0B, MIO1T, MIO1B . . . MIO255T, MIO255B)are read into the data registers RE. During restoring, the restoring signal RS is activated, and data items in the data registers RE are written in the sense amplifiers SA over the main input/output lines MIO. Moreover, the data items are written in the memory cells MC, which are interconnected over a selected word line, by way of the bit lines.

Please replace paragraph [0060] with the following amended paragraph:

In addition, the internal node REI0B of the data register is connected onto a global input/output line GIO via a column selecting switch NMOS transistor MN5. A column selection line YS (YS0, YS1 . . .YS255) is connected to the gate of the NMOS transistor MN5. During reading or writing, column selection lines YS associated with desired addresses are successively selected, and the data registers RE are successively connected onto the global input/output line GIO. Data items are then received or transmitted.

Please replace paragraph [0061] with the following amended paragraph:

The flag register FRE has the same circuit elements as the data registers RE such as MIOFT, MIOFB, FREB, FRET and MN6. However, since the flag register FRE performs pre-fetching earlier than the data registers do, the flag register FRE has an independent input clock PFF. The group number register BN performs reading alone and, therefore, has an input switch alone, but does not have the clocked inverters CIV1 and CIV3 and column selecting switch NMOS transistor which are included in the flag register FRE. The output nodes are BN0, BN1, and BN is connected to main input/output lines MIONT and MIONB. As shown in Fig. 4, the NMOS transistor MN6 included in the flag register FRE is connected onto a terminal FREW over a flag column selection line YSF coupled to the gate thereof.

Please replace paragraph [0066] with the following amended paragraph:

Fig. 6 shows waveforms relevant to actions performed in the encoding control circuit ENCNTL. When a group of memory cells is selected based on a received Pre-fetch ~~command~~ COMMAND PFC, data items are read from the sense amplifiers associated with the group of memory cells and placed on the data main input/output lines MIO0 (MIO0B, MIO0T) and the flag main input/output line MIOF (MIOFT, MIOFB), respectively.

Please replace paragraph [0067] with the following amended paragraph:

The flag input clock PFF is activated first, and the data placed on the flag main input/output line MIOF is read into the flag register FRE. Moreover, the data placed on the group number register main input/output line MION is read into the group number register BN (BN0, BN1). Based on the flag, the encoders EN selects one of the polarities to be switched. Referring to Fig. 6, the flag recorded in the flag register FRE is set to a 1 (the node FRET is driven high and the node FREB is driven low). The data items on the data main input/output lines MIO are therefore inverted and read into the data registers RE. Referring to Fig. 6, the main input/output lines MIO0T and MIO0B and the data register input/output lines REIO (REIOT, REIOB)~~REI0T and REI0B~~ make a low-to-high or high-to-low transition.

Please replace paragraph [0068] with the following amended paragraph:

The encoding control circuit ENCNTL receives a Write command WRT. Every time the contents of the data registers RE are rewritten, a counter-activating signal CNTE is activated. It is then determined whether the number of 1s or the number of 0s is larger. The flag column selection line YSF is then activated in order to update the flag recorded in the flag register FRE from terminal FREW. During restoring (RST), the data items in the data registers RE are inverted or non-inverted based on the flag recorded in the flag register FRE, and then placed on the main input/output lines MIO. At the same time, the flag in the flag register FRE is written in the associated sense amplifier and memory cell over the flag main input/output line MIOF. Restoring signal RS is also activated.

Please replace paragraph [0069] with the following amended paragraph:

Fig. 7 shows an example of the circuitry of another preferred embodiment of the present invention comprising a register-incorporated DRAM. The actions to be performed in the DRAM of this preferred embodiment are described below. An address signal ADD is transmitted to an address buffer ADDBUF. A chip selecting signal /CS, a row address strobe signal /RAS, a column address strobe signal /CAS, and a writing enabling signal /WE are transmitted to a command decoder COMDEC. A clock CLK and a clock-enabling signal CKE are transmitted to a clock generator CLKGEN. The command decoder COMDEC decodes a received control signal and determines an operation mode by selecting any of a reading mode, a writing mode, and a pre-charging mode. A control logic LOGIC produces control signals required depending on the operation mode within a chip. A mode register MDREG holds a current operation mode. Register controller REGCNTL receives a signal from address buffer ADDBUF and controls the register selecting decoder RESEL.

Please replace paragraph [0073] with the following amended paragraph:

Moreover, when the number of registers belonging to one data register bank REB is large, if data items placed on a plurality of word lines are simultaneously read into one register bank, data items placed on the same word line are grouped into a sub-block. The encoding described in conjunction with Fig. 1 is performed on each sub-block, and a flag memory cell (FLG) is created for each sub-block.